FIG.1

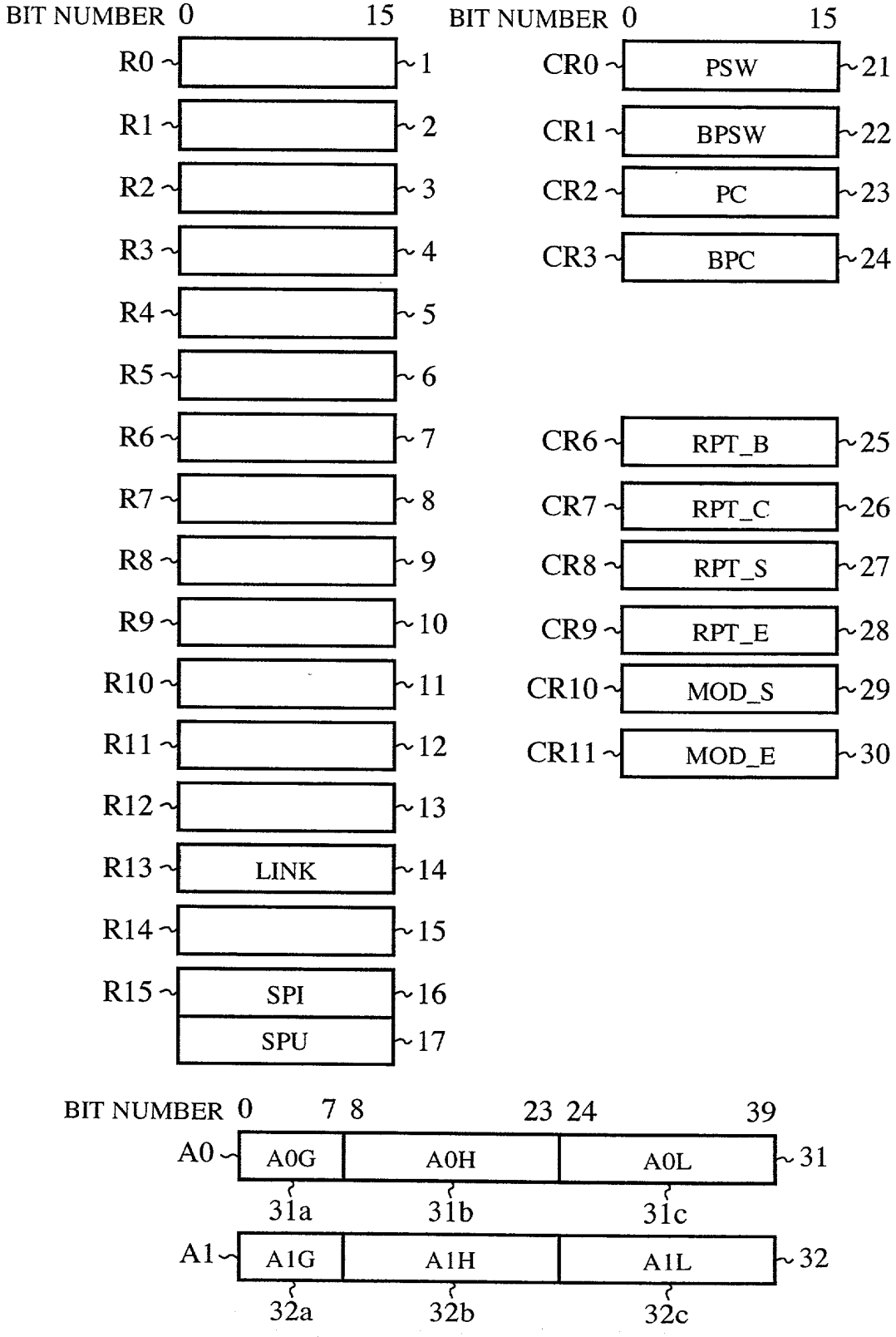
BIT NUMBER 0 15
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
LINK
R14
R15
SPI
SPU
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
BIT NUMBER 0 15
CR0
PSW
CR1
BPSW
CR2
PC
CR3
BPC
CR6
RPT_B
CR7
RPT_C
CR8
RPT_S
CR9
RPT_E
CR10
MOD_S
CR11
MOD_E
21
22
23
24
25
26
27
28
29
30
BIT NUMBER 0 7 8 23 24 39
A0
A0G
A0H
A0L
31
31a
31b
31c
A1
A1G
A1H
A1L
32
32a
32b
32c

FIG.2

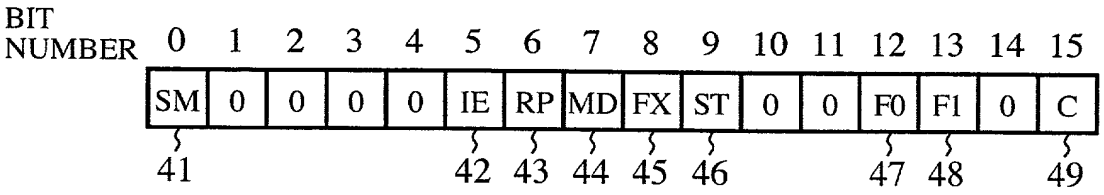

FIG.3

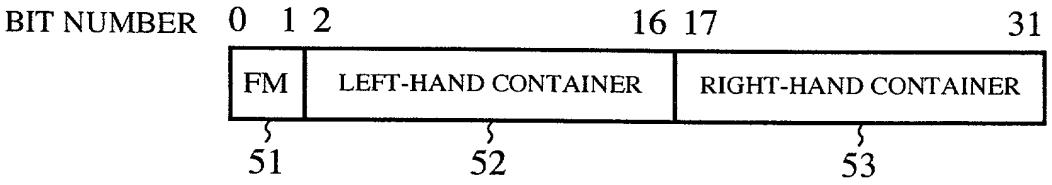

FIG.4

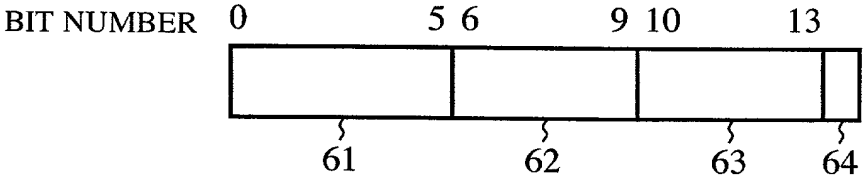

FIG.5

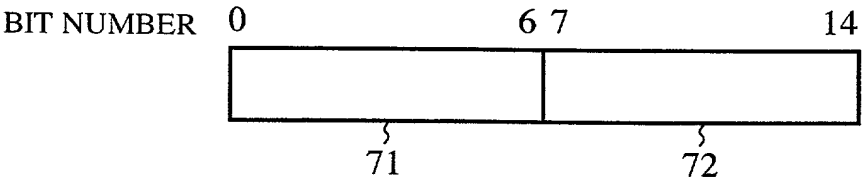

FIG.6

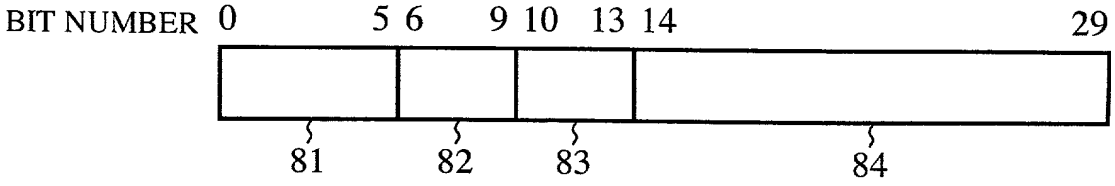
BIT NUMBER
0
5 6
9 10
13 14
29
81
82
83
84

FIG.7

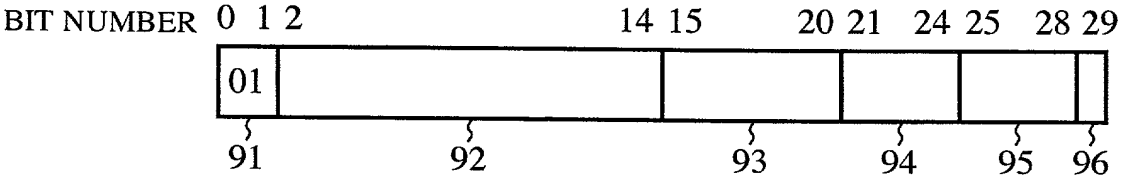
BIT NUMBER
0 1 2
14 15
20 21
24 25
28 29
01
91
92
93
94
95
96

FIG.8

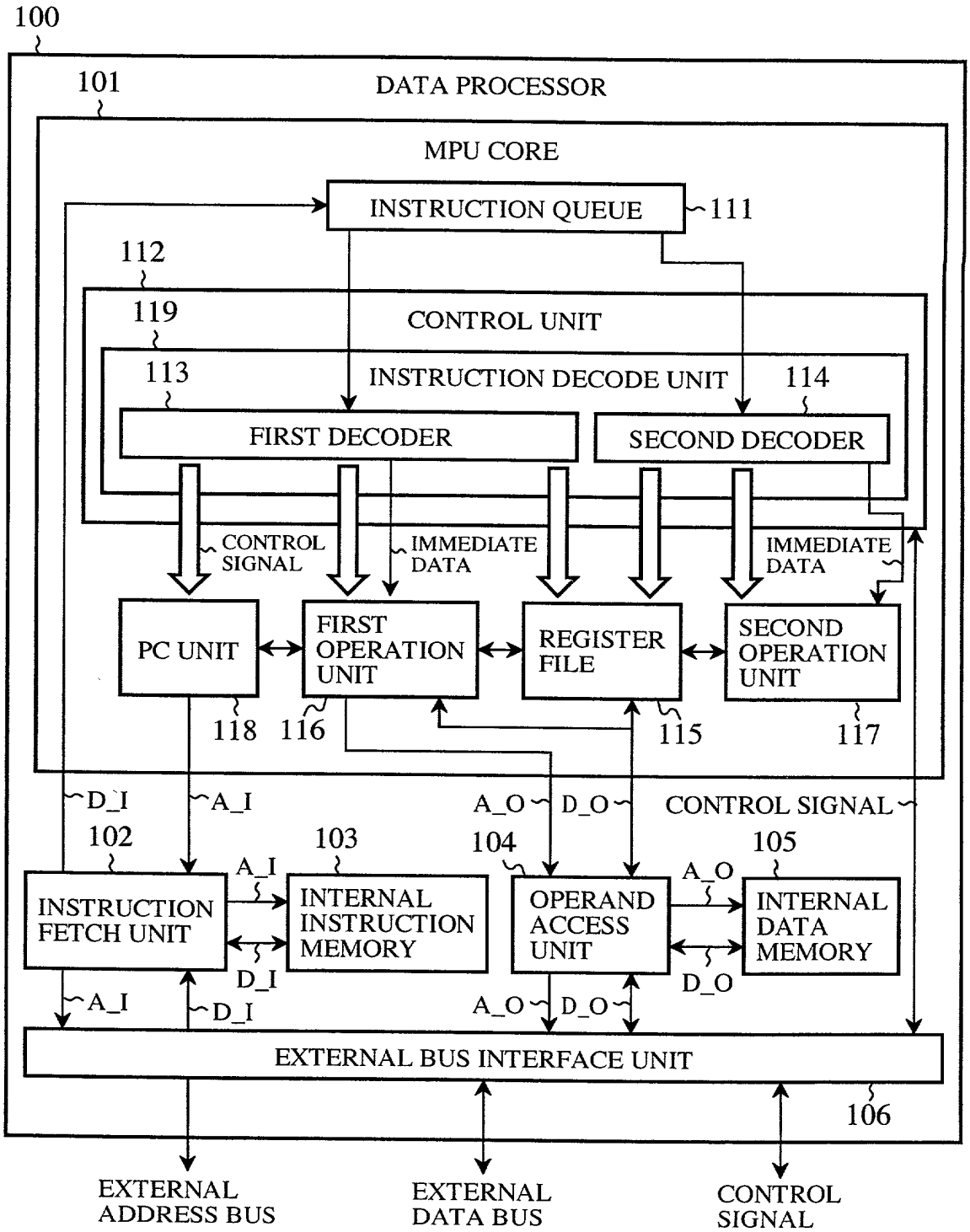
100
101
DATA PROCESSOR
MPU CORE
INSTRUCTION QUEUE
111
112
119
CONTROL UNIT
113
INSTRUCTION DECODE UNIT
114
FIRST DECODER
SECOND DECODER
CONTROL SIGNAL
IMMEDIATE DATA
IMMEDIATE DATA
PC UNIT
FIRST OPERATION UNIT
REGISTER FILE
SECOND OPERATION UNIT
118
116
115
117
D_I
A_I
A_O
D_O
CONTROL SIGNAL
102
103
104
105
A_I
A_O
INSTRUCTION FETCH UNIT
INTERNAL INSTRUCTION MEMORY
OPERAND ACCESS UNIT
INTERNAL DATA MEMORY
D_I
D_O
A_I
D_I
A_O
D_O
EXTERNAL BUS INTERFACE UNIT
106
EXTERNAL ADDRESS BUS
EXTERNAL DATA BUS
CONTROL SIGNAL

FIG.9

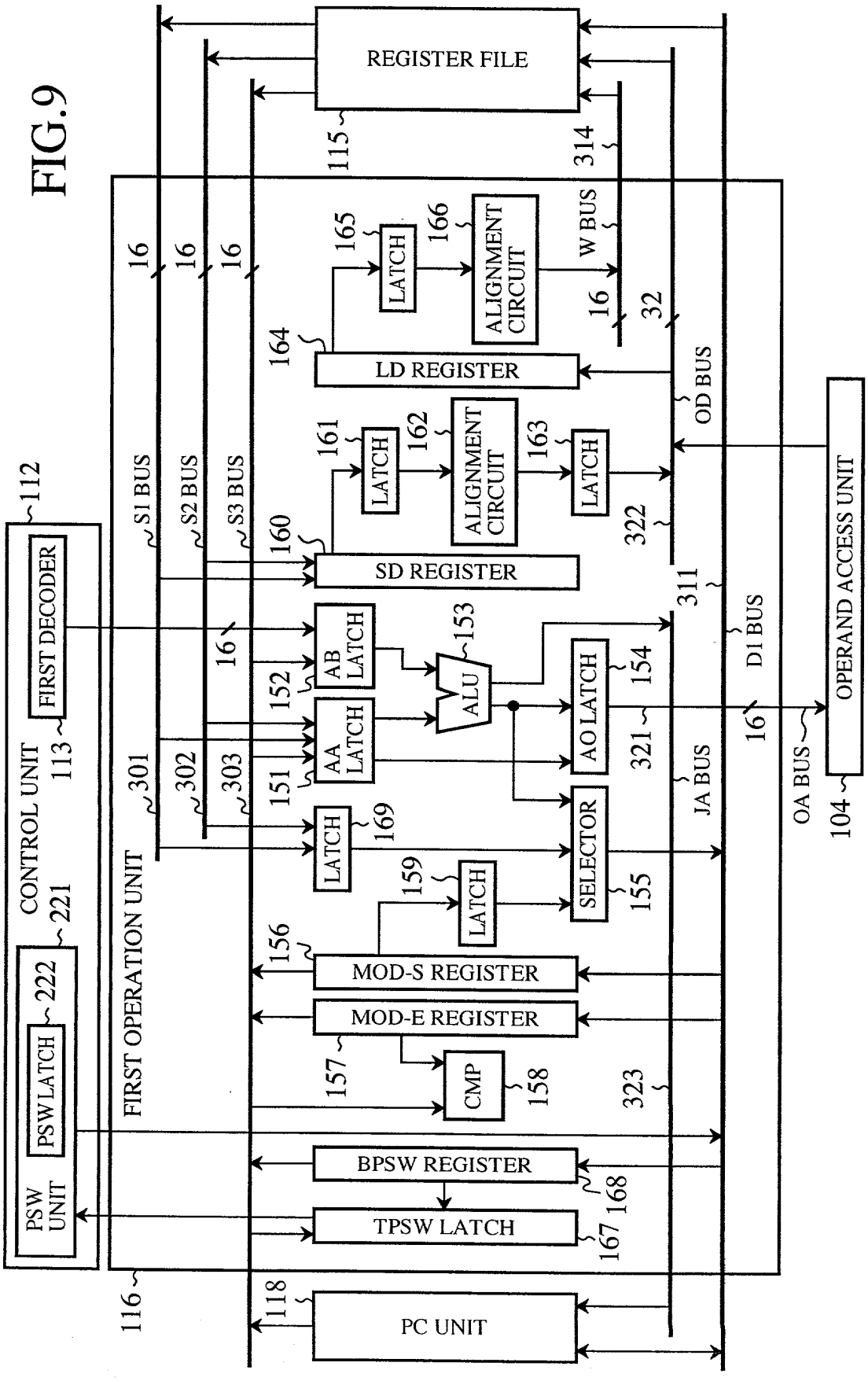
REGISTER FILE
115
314
W BUS
165
LATCH
166
ALIGNMENT CIRCUIT
16
32
164
LD REGISTER
OD BUS
161
LATCH
162
ALIGNMENT CIRCUIT
163
LATCH
322
160
SD REGISTER
311
D1 BUS
OPERAND ACCESS UNIT
104
OA BUS
112
CONTROL UNIT
113
FIRST DECODER
S1 BUS
S2 BUS
S3 BUS
16
AB LATCH
153
ALU
154
AO LATCH
152
AA LATCH
151
301
302
303
321
JA BUS
LATCH
169
159
LATCH
SELECTOR
155
156
MOD-S REGISTER
MOD-E REGISTER
157
CMP
158
323
221
PSW LATCH
222
PSW UNIT
FIRST OPERATION UNIT
BPSW REGISTER
168
TPSW LATCH
167
116
118
PC UNIT

FIG.10

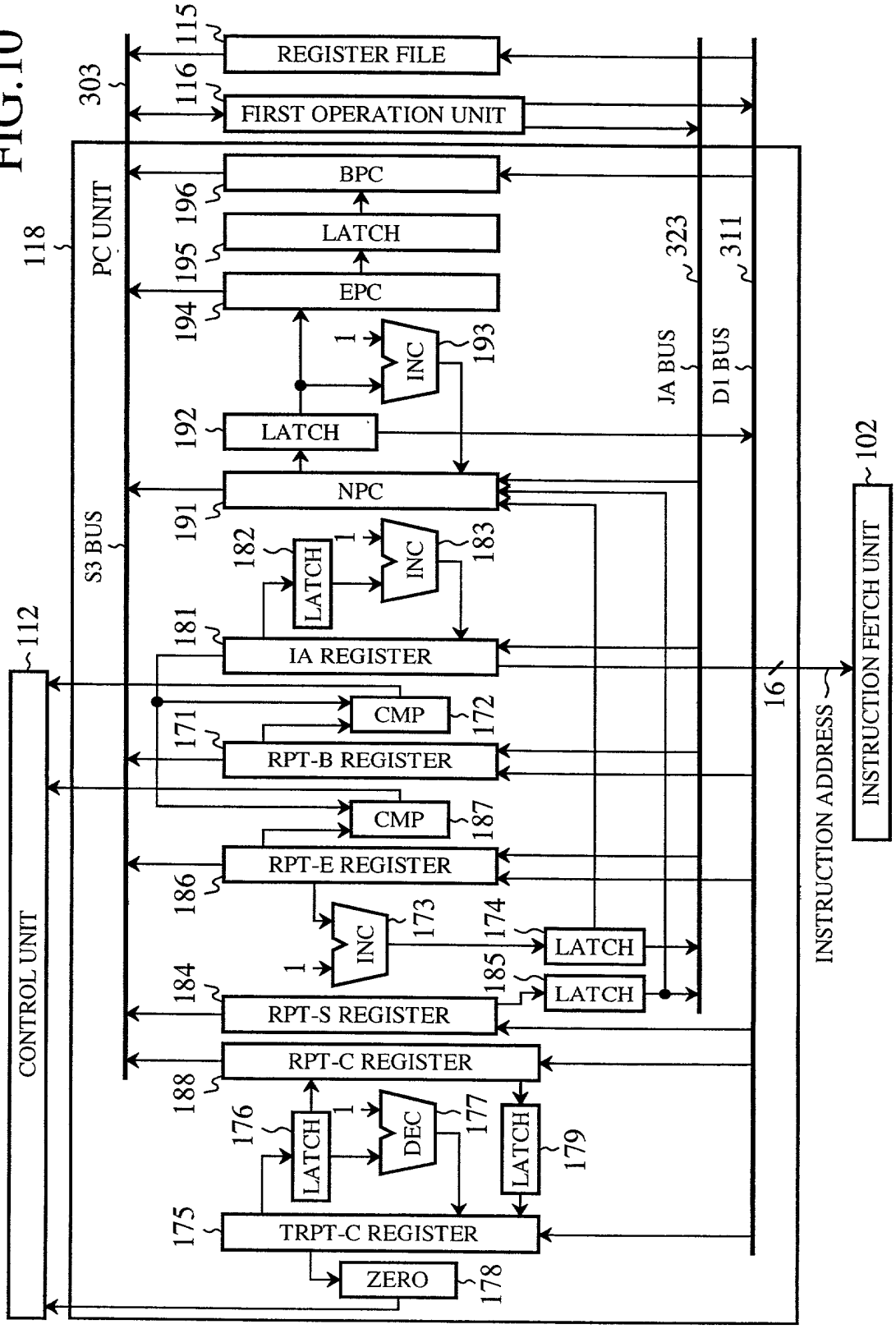
REGISTER FILE
FIRST OPERATION UNIT
BPC
LATCH
EPC
INC
LATCH
NPC
LATCH
INC
IA REGISTER
CMP
RPT-B REGISTER
CMP
RPT-E REGISTER
INC
LATCH
LATCH
RPT-S REGISTER
RPT-C REGISTER
LATCH
DEC
LATCH
TRPT-C REGISTER
ZERO
PC UNIT
S3 BUS
JA BUS
D1 BUS
CONTROL UNIT
INSTRUCTION ADDRESS
INSTRUCTION FETCH UNIT
303
115
116
118
196
195
194
193
192
191
182
183
181
112
171
172
187
186
173
174
184
185
188
176
177
179
175
178
323
311
102
16

FIG.11

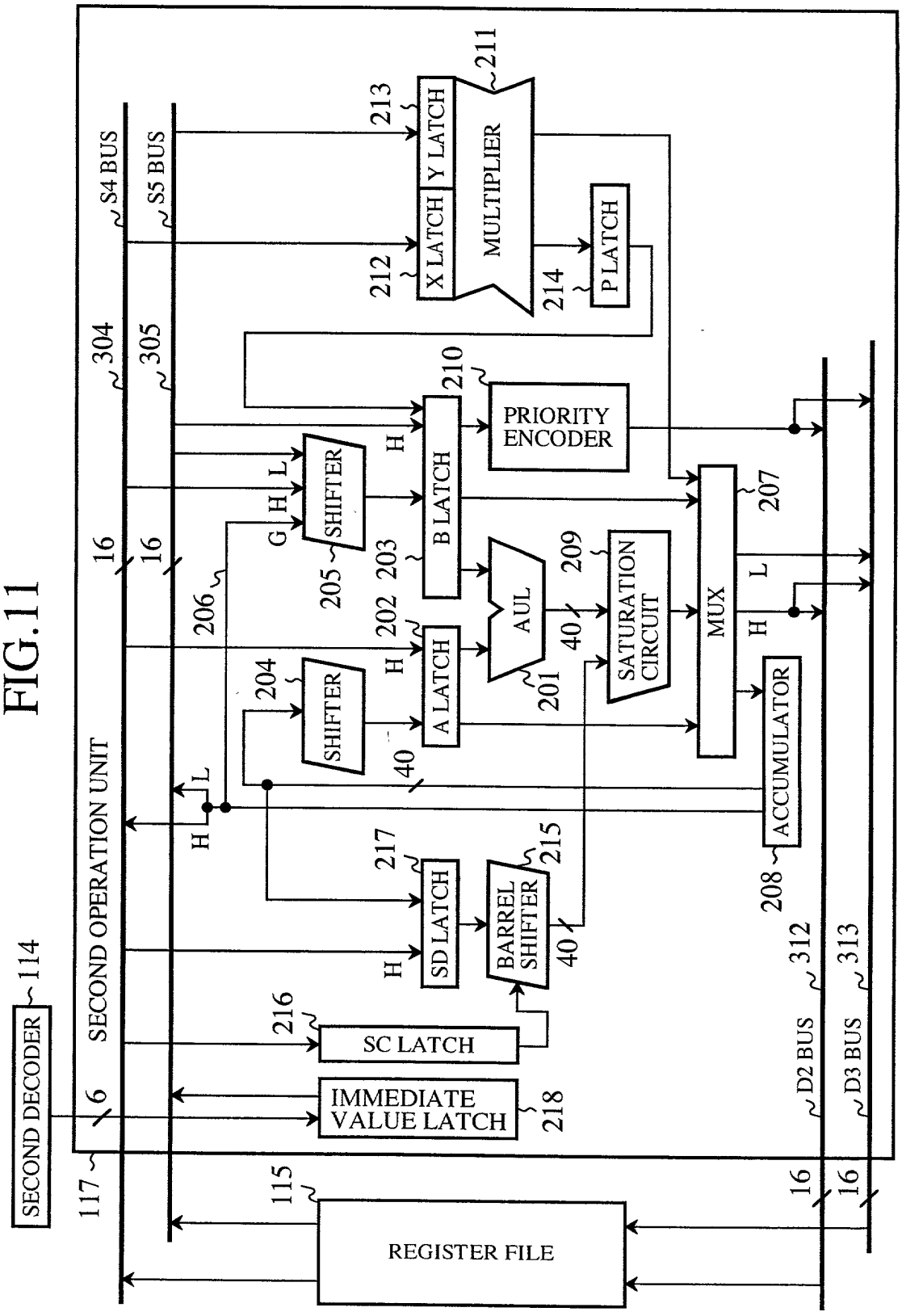
SECOND DECODER
114
SECOND OPERATION UNIT
6
117
115
REGISTER FILE
S4 BUS
S5 BUS
304
305
16
16
213
X LATCH
Y LATCH
MULTIPLIER
211
212
214
P LATCH
210
PRIORITY ENCODER
H
B LATCH
203
205
G
H
L
SHIFTER
206
202
A LATCH
204
SHIFTER
AUL
201
209
SATURATION CIRCUIT
40
MUX
207
H
L
ACCUMULATOR
208
H
L
40
217
SD LATCH
215
BARREL SHIFTER
40
216
SC LATCH
IMMEDIATE VALUE LATCH
218
312
313
D2 BUS
D3 BUS
16
16

FIG.12

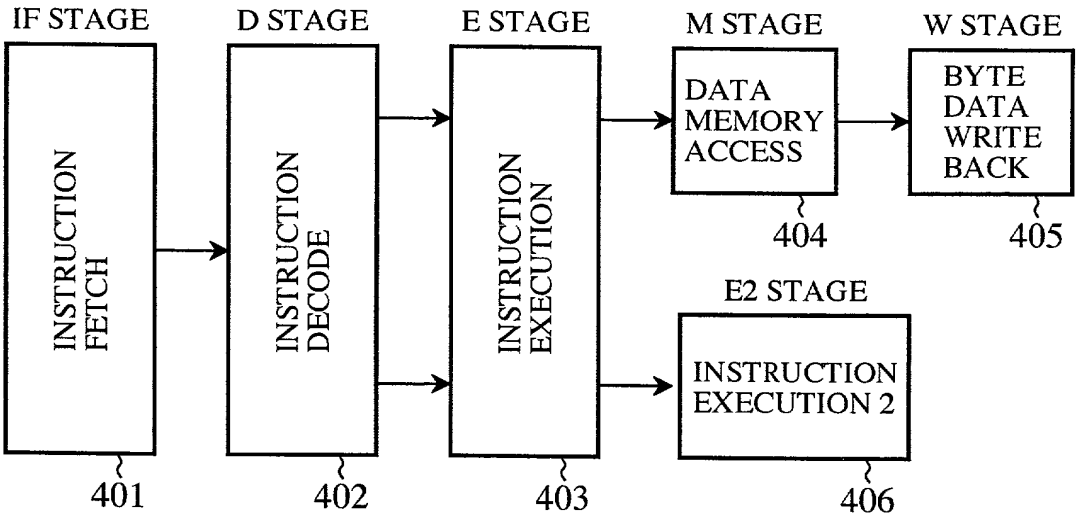

FIG.13

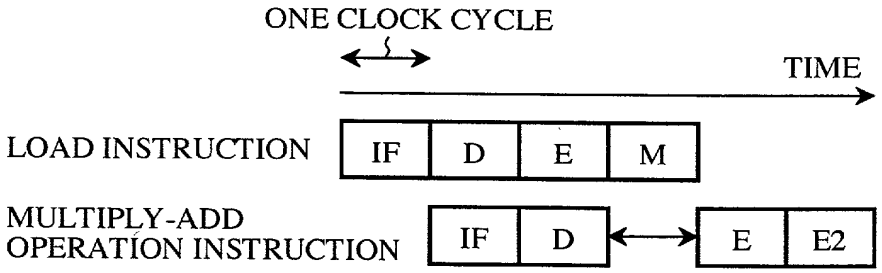

FIG.14

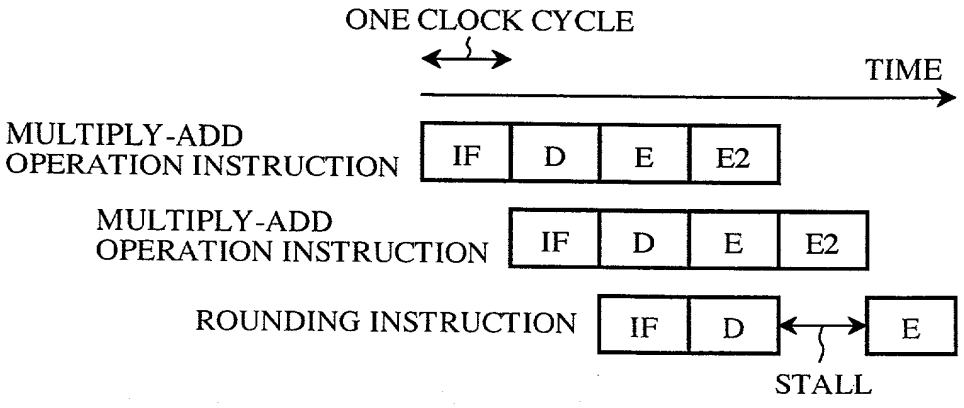

FIG.15

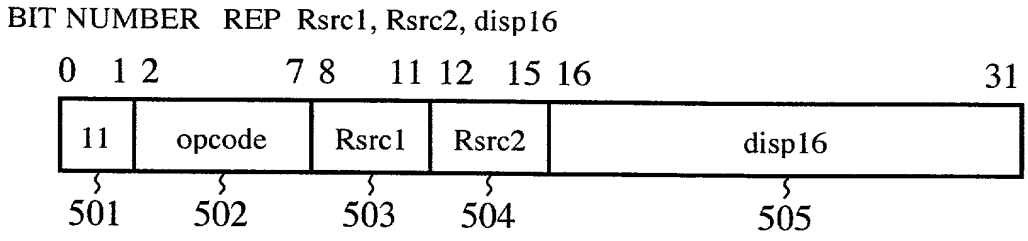

FIG.16

```
  AND3    R11,R10,#h'0003                          ; I1
  LD2W    R0,@R8+     ||  SRLI    R10,#2           ; I2
  LD2W    R4,@R9+     ||  NOP                      ; I3
  LD2W    R2,@R8+     ||  CLRAC   A0               ; I4

  REP     R11,R10,rep_end                          ; I5

  LD2W    R6,@R9+     ||  MAC     A0,R0,R4         ; I6
  LD2W    R0,@R8+     ||  MAC     A0,R1,R5         ; I7
  LD2W    R4,@R9+     ||  MAC     A0,R2,R6         ; I8
rep_end :
  LD2W    R2,@R8+     ||  MAC     A0,R3,R7         ; I9

  RACHI   R0,A0,#0    ||  NOP                      ; I10
  :                                                ; I11
  :                                                ; :
```

FIG.17

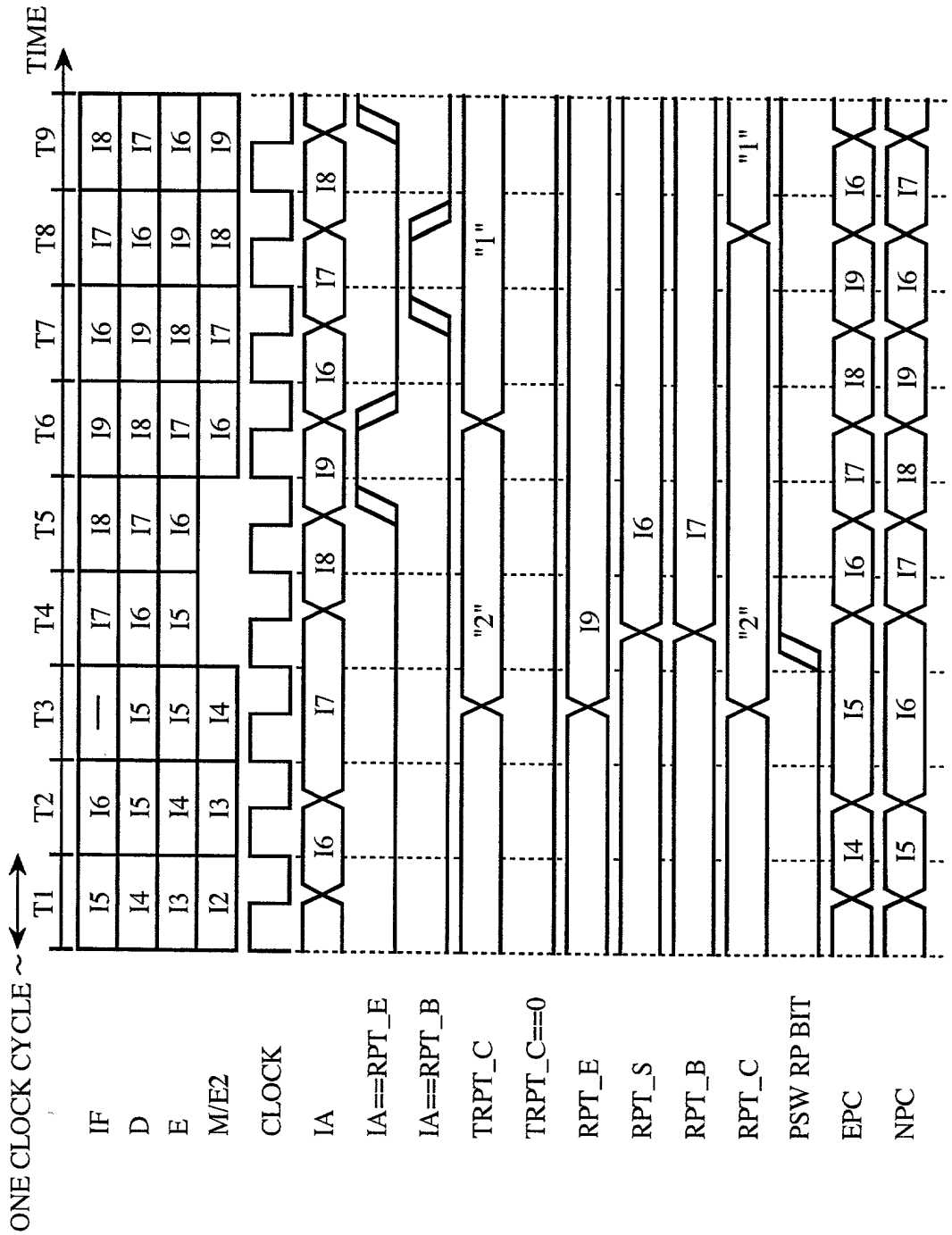
ONE CLOCK CYCLE
T1
T2
T3
T4
T5
T6
T7
T8
T9
TIME
IF
D
E
M/E2
CLOCK
IA
IA==RPT_E
IA==RPT_B
TRPT_C
TRPT_C==0
RPT_E
RPT_S
RPT_B
RPT_C
PSW RP BIT
EPC
NPC
"1"
"2"

FIG.18

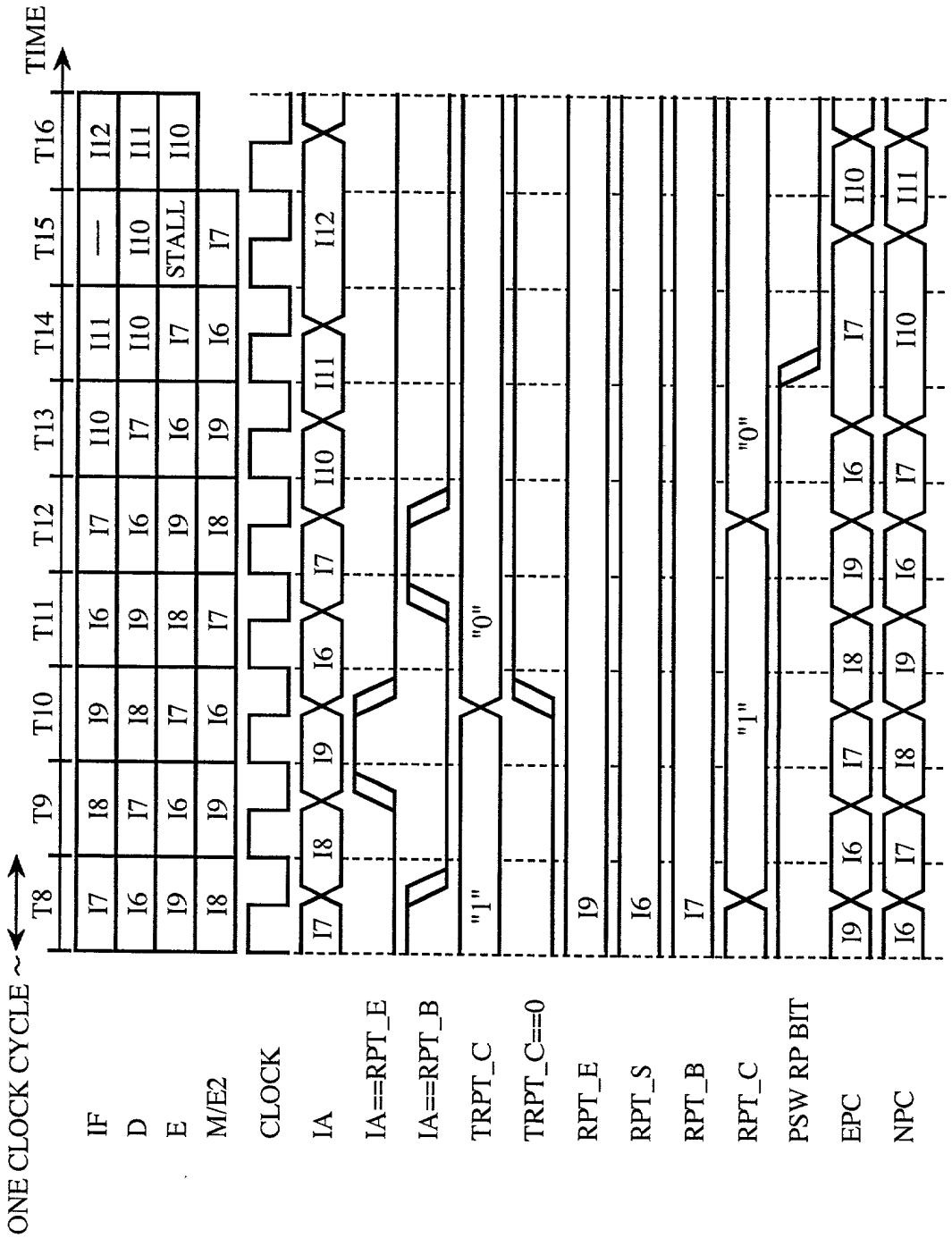
ONE CLOCK CYCLE
T8
T9
T10
T11
T12
T13
T14
T15
T16
TIME
IF
D
E
M/E2
CLOCK
IA
IA==RPT_E
IA==RPT_B
TRPT_C
TRPT_C==0
RPT_E
RPT_S
RPT_B
RPT_C
PSW RP BIT
EPC
NPC
I7 I8 I9 I6 I7 I10 I11 — I12
I6 I7 I8 I9 I6 I7 I10 I11 I12
I9 I6 I7 I8 I9 I6 I7 I10 I11
I8 I9 I6 I7 I8 I9 I6 I7 STALL I10
"1"
"0"
"1"
"0"
I9
I6
I7
I9 I6 I7 I8 I9 I6 I7 I10
I6 I7 I8 I9 I6 I7 I10 I11

FIG.19

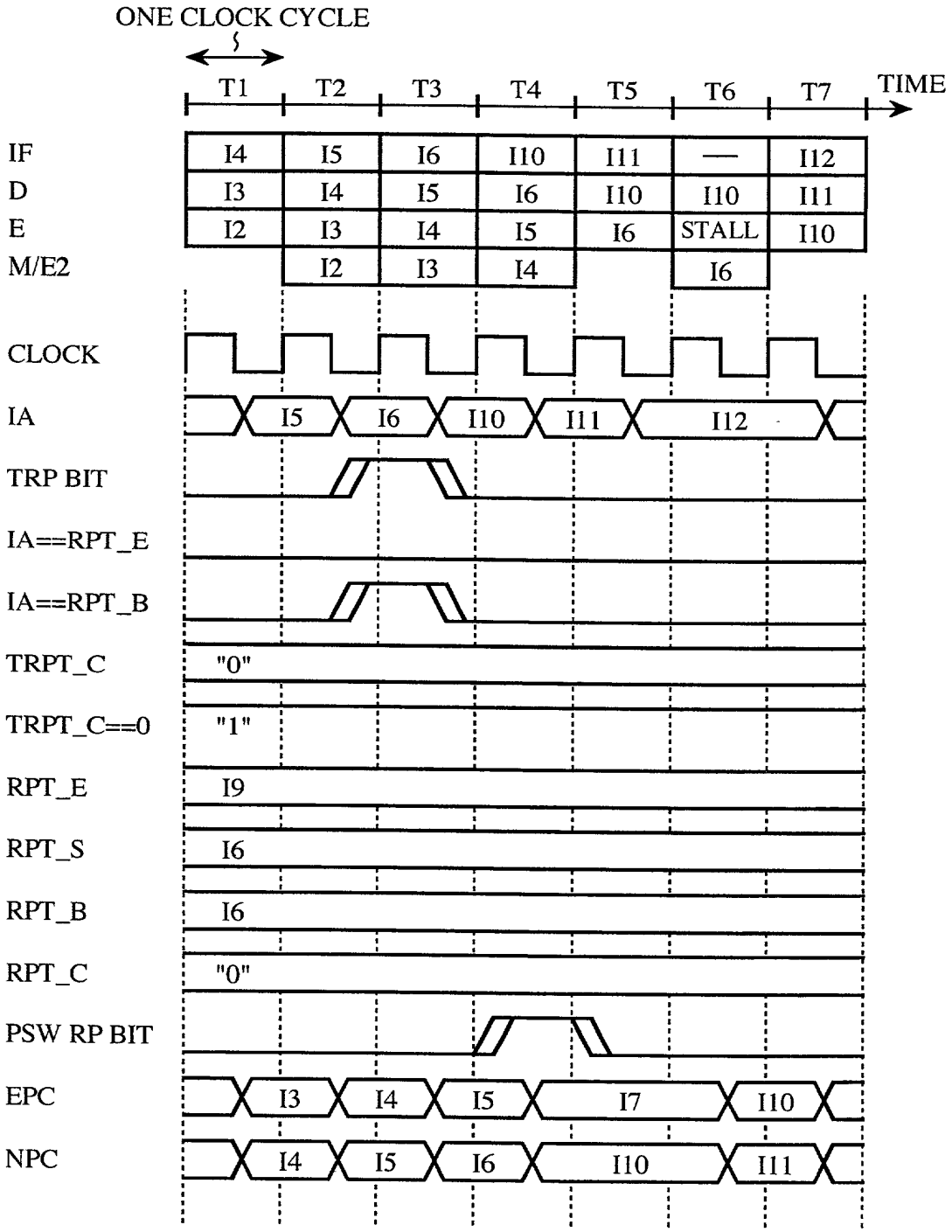
ONE CLOCK CYCLE
T1
T2
T3
T4
T5
T6
T7
TIME
IF
D
E
M/E2
I4
I5
I6
I10
I11
—
I12
I3
I4
I5
I6
I10
I10
I11
I2
I3
I4
I5
I6
STALL
I10
I2
I3
I4
I6
CLOCK
IA
I5
I6
I10
I11
I12
TRP BIT
IA==RPT_E
IA==RPT_B
TRPT_C
"0"
TRPT_C==0
"1"
RPT_E
I9
RPT_S
I6
RPT_B
I6
RPT_C
"0"
PSW RP BIT
EPC
I3
I4
I5
I7
I10
NPC
I4
I5
I6
I10
I11

FIG.20

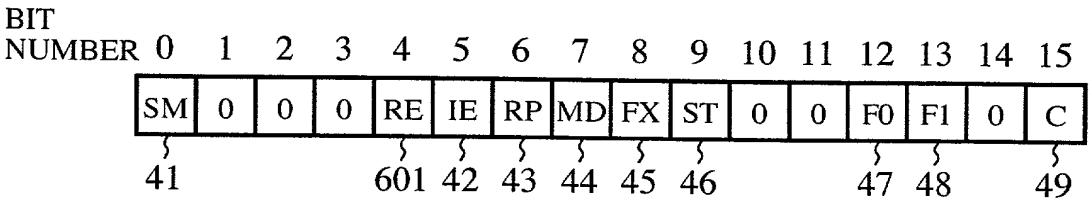

FIG.25

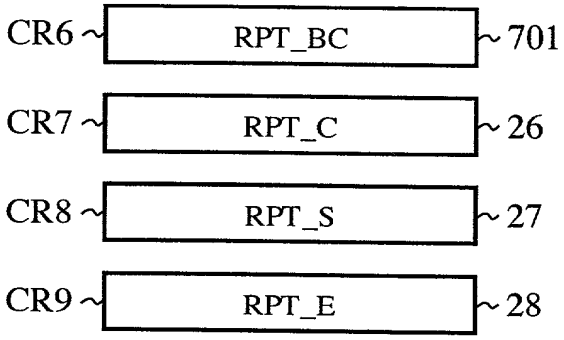

FIG.29

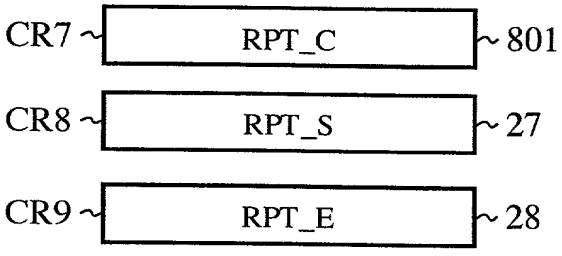

FIG.21

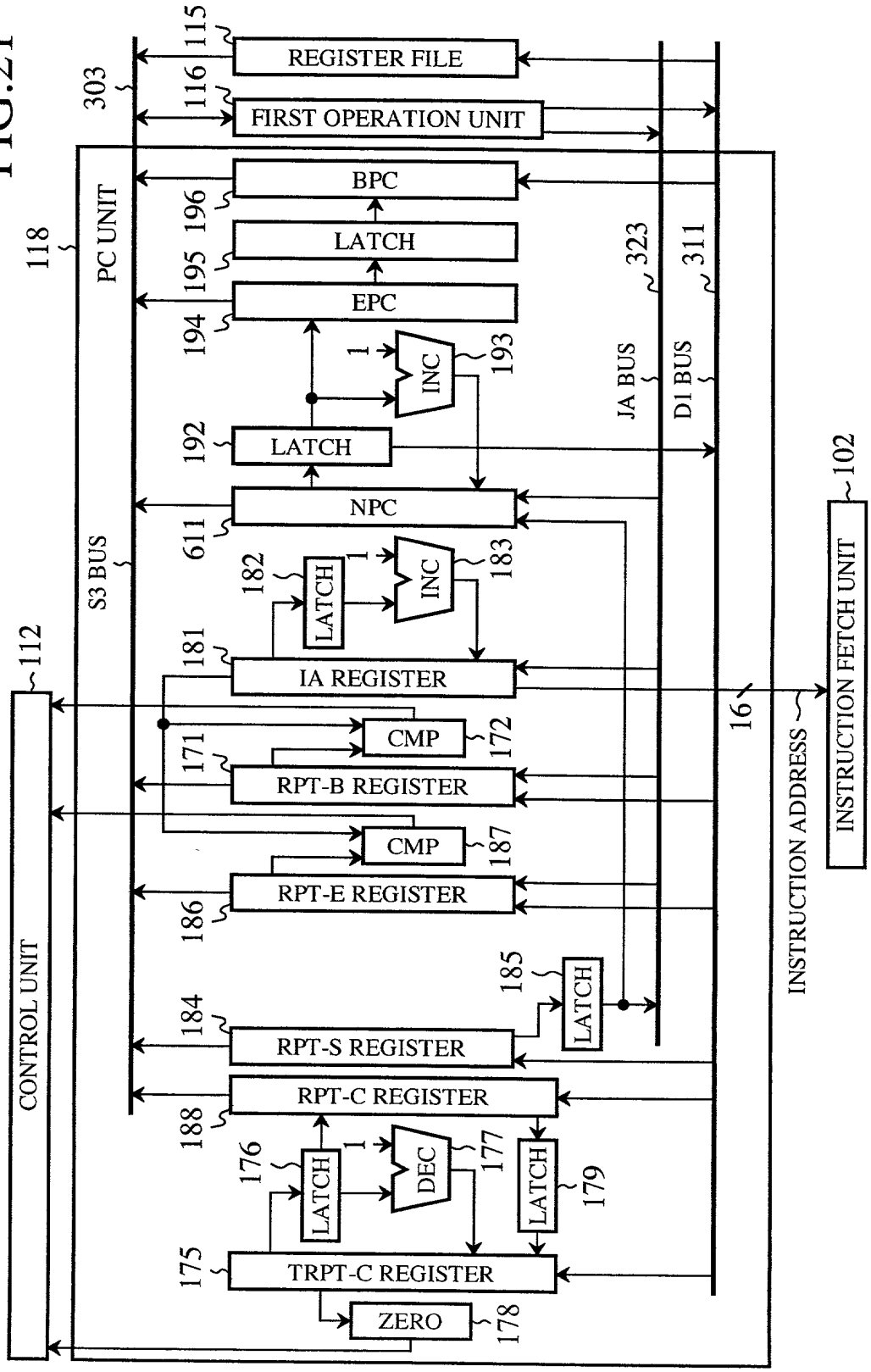
REGISTER FILE
FIRST OPERATION UNIT
BPC
LATCH
EPC
INC
LATCH
NPC
LATCH
INC
IA REGISTER
CMP
RPT-B REGISTER
CMP
RPT-E REGISTER
LATCH
RPT-S REGISTER
RPT-C REGISTER
LATCH
DEC
LATCH
TRPT-C REGISTER
ZERO
PC UNIT
S3 BUS
JA BUS
D1 BUS
CONTROL UNIT
INSTRUCTION ADDRESS
INSTRUCTION FETCH UNIT
303
115
116
118
196
195
194
193
192
611
182
183
181
112
171
172
187
186
185
184
188
176
177
179
175
178
323
311
16
102

FIG.22

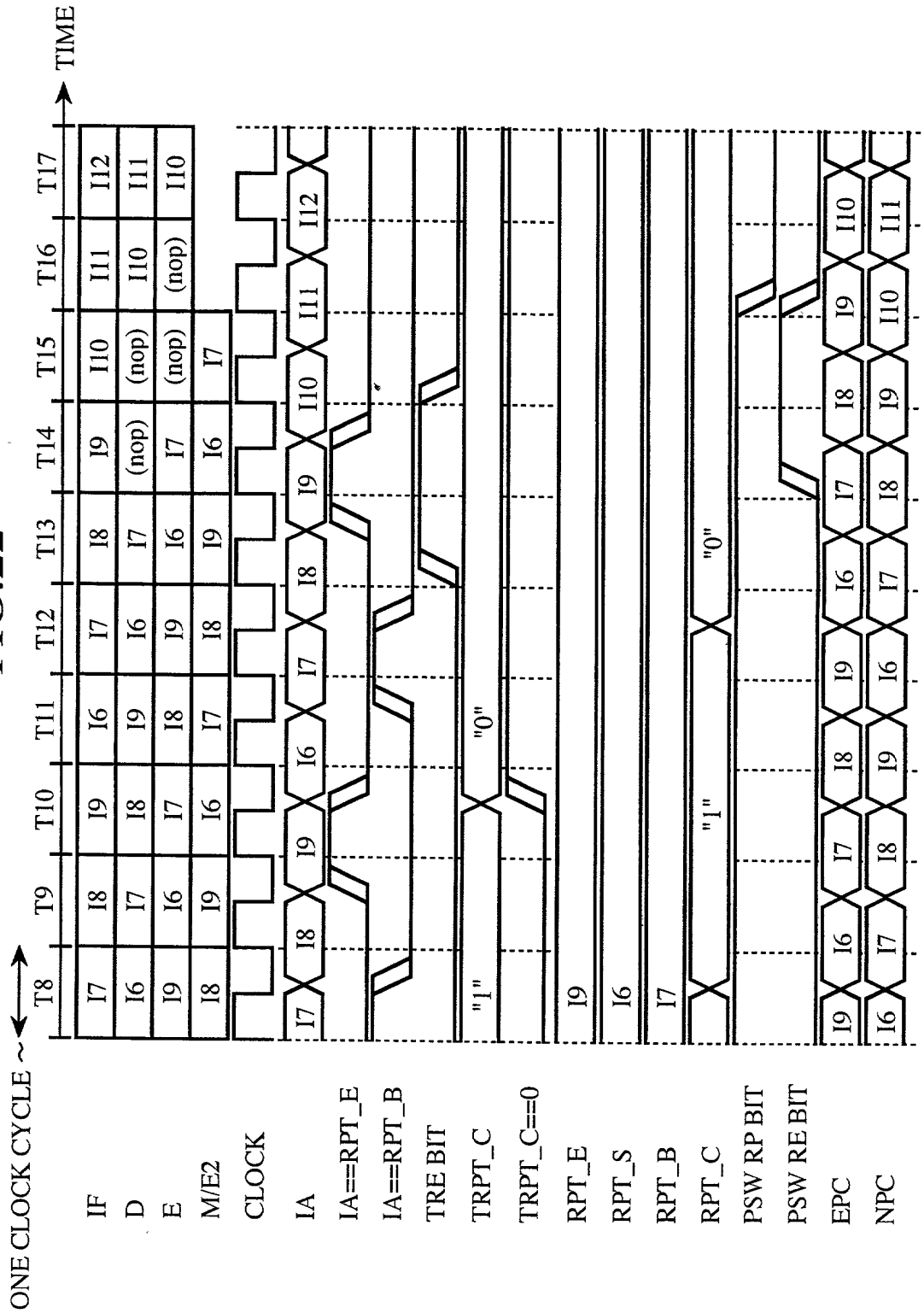
ONE CLOCK CYCLE
TIME
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
IF
D
E
M/E2
CLOCK
IA
IA==RPT_E
IA==RPT_B
TRE BIT
TRPT_C
TRPT_C==0
RPT_E
RPT_S
RPT_B
RPT_C
PSW RP BIT
PSW RE BIT
EPC
NPC
I7 I8 I9 I6 I7 I8 I9 I10 I11 I12
I6 I7 I8 I9 I6 I7 I8 I9 I10 I11
I9 I6 I7 I8 I9 I6 I7 (nop) (nop) (nop)
I8 I9 I6 I7 I8 I9 I6 I7
"1"
"0"
"1"
"0"
I9
I6
I7
I9 I6 I7 I8 I9 I6 I7 I8 I9 I10
I6 I7 I8 I9 I6 I7 I8 I9 I10 I11

FIG.23

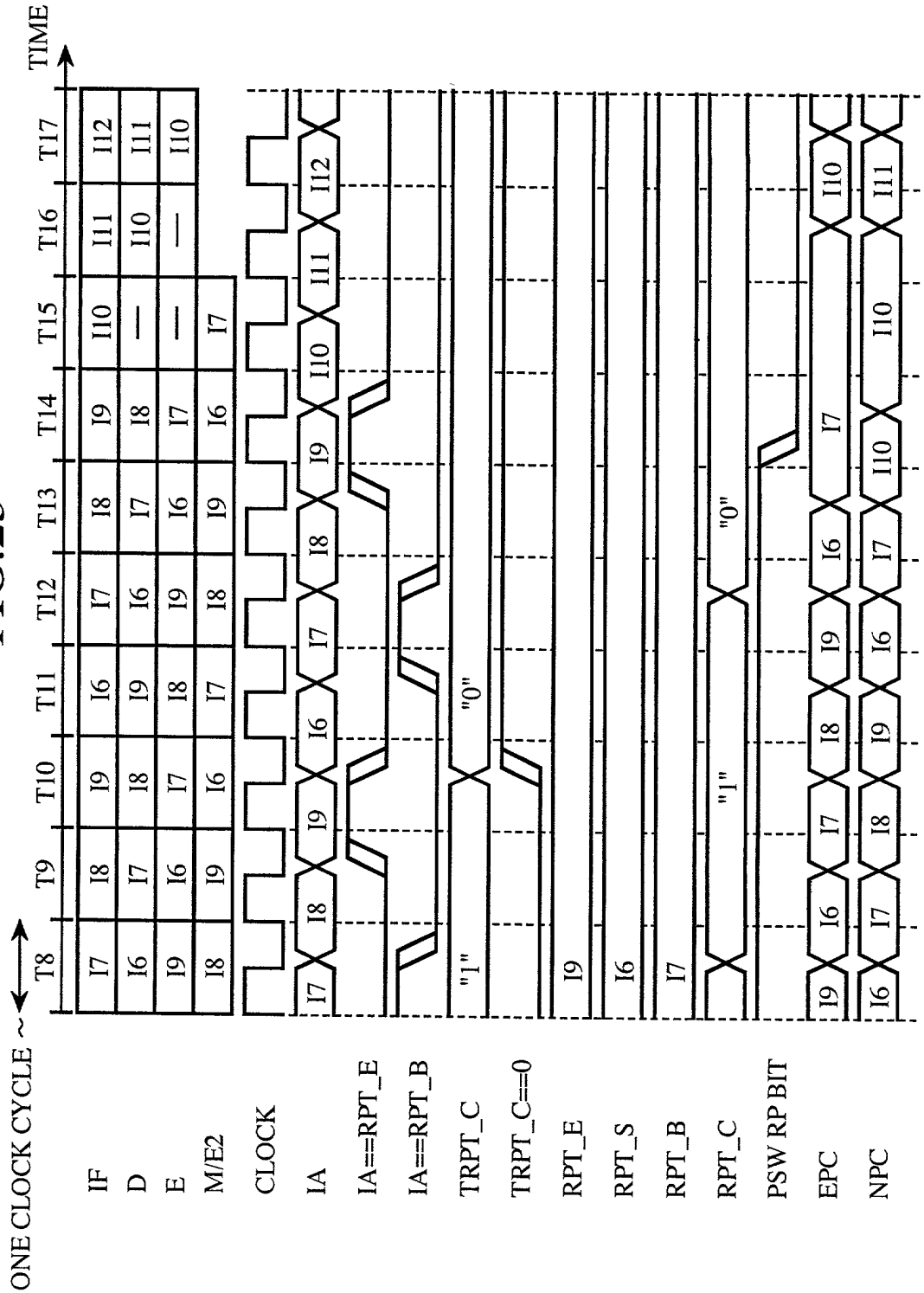
TIME
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
ONE CLOCK CYCLE
IF
D
E
M/E2
CLOCK
IA
IA==RPT_E
IA==RPT_B
TRPT_C
TRPT_C==0
RPT_E
RPT_S
RPT_B
RPT_C
PSW RP BIT
EPC
NPC
"1"
"0"

FIG.24

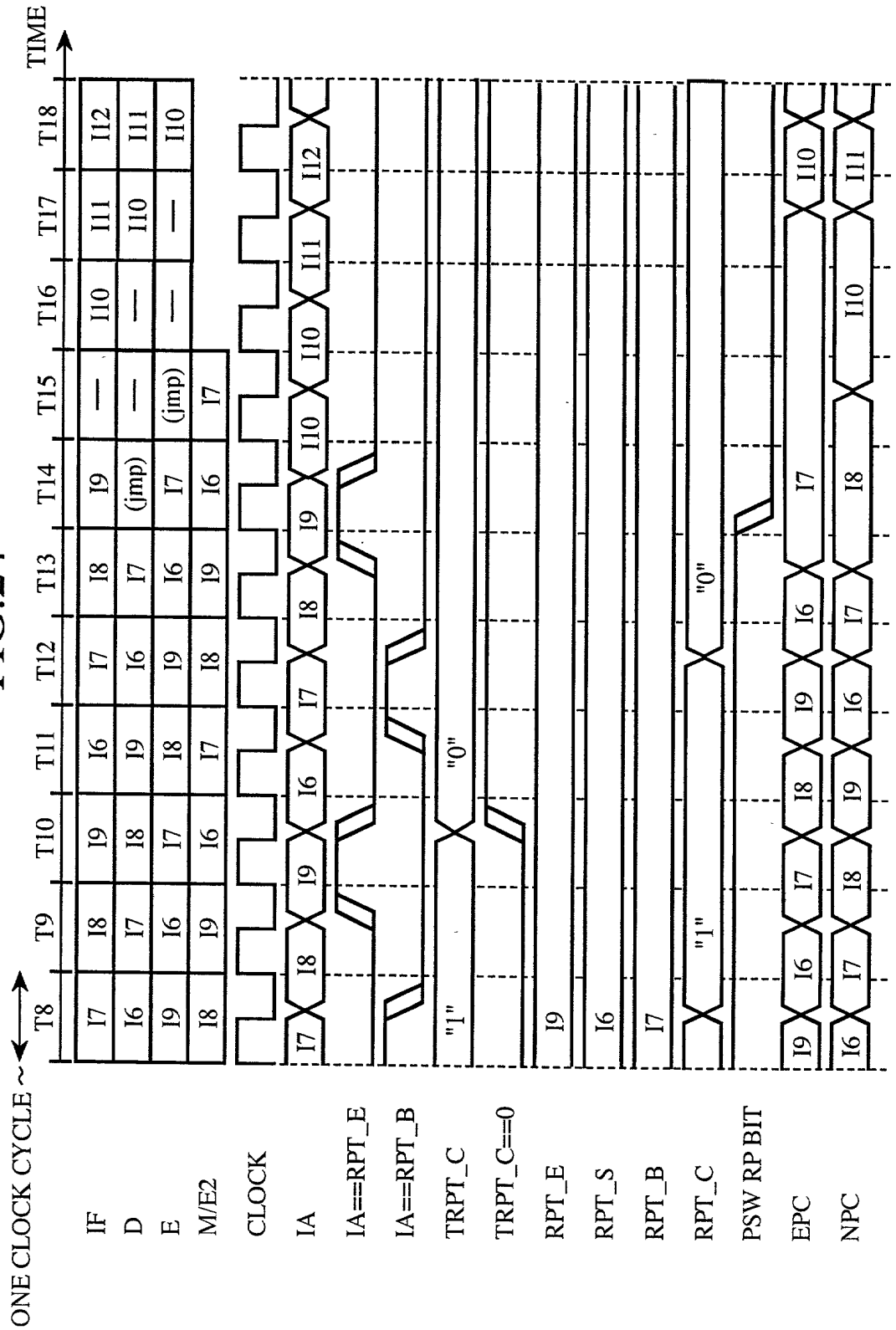
TIME
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
ONE CLOCK CYCLE
IF
D
E
M/E2
CLOCK
IA
IA==RPT_E
IA==RPT_B
TRPT_C
TRPT_C==0
RPT_E
RPT_S
RPT_B
RPT_C
PSW RP BIT
EPC
NPC
(jmp)
"0"
"1"

FIG.26

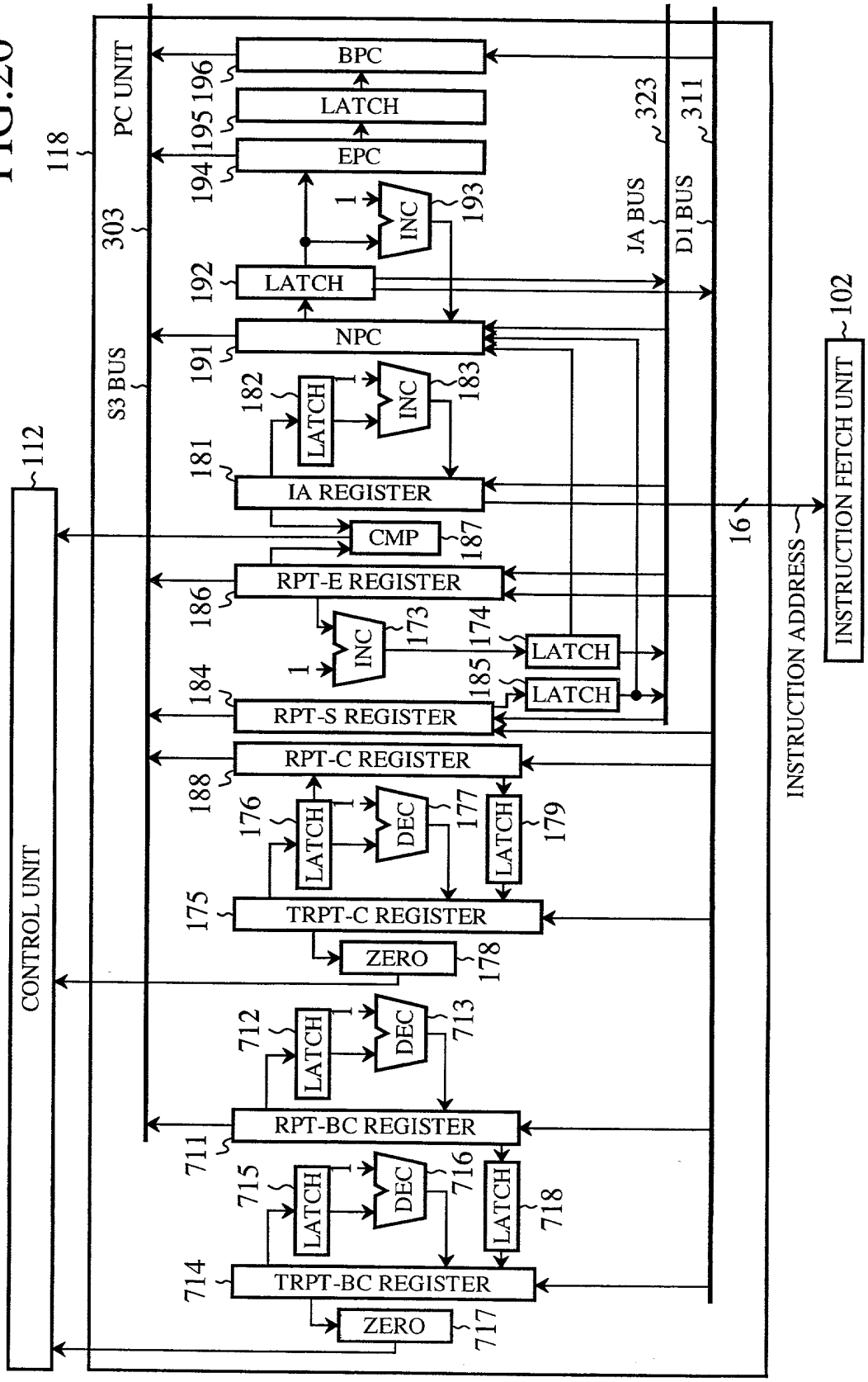
PC UNIT
118
BPC
196
LATCH
195
EPC
194
INC
193
1
LATCH
192
NPC
191
LATCH
182
INC
183
1
IA REGISTER
181
CMP
187
RPT-E REGISTER
186
INC
173
1
174
LATCH
185
LATCH
RPT-S REGISTER
184
RPT-C REGISTER
188
LATCH
176
DEC
177
LATCH
179
TRPT-C REGISTER
175
ZERO
178
LATCH
712
DEC
713
RPT-BC REGISTER
711
LATCH
715
DEC
716
LATCH
718
TRPT-BC REGISTER
714
ZERO
717
S3 BUS
303
JA BUS
323
D1 BUS
311
CONTROL UNIT
112
16
INSTRUCTION ADDRESS
INSTRUCTION FETCH UNIT
102

FIG.27

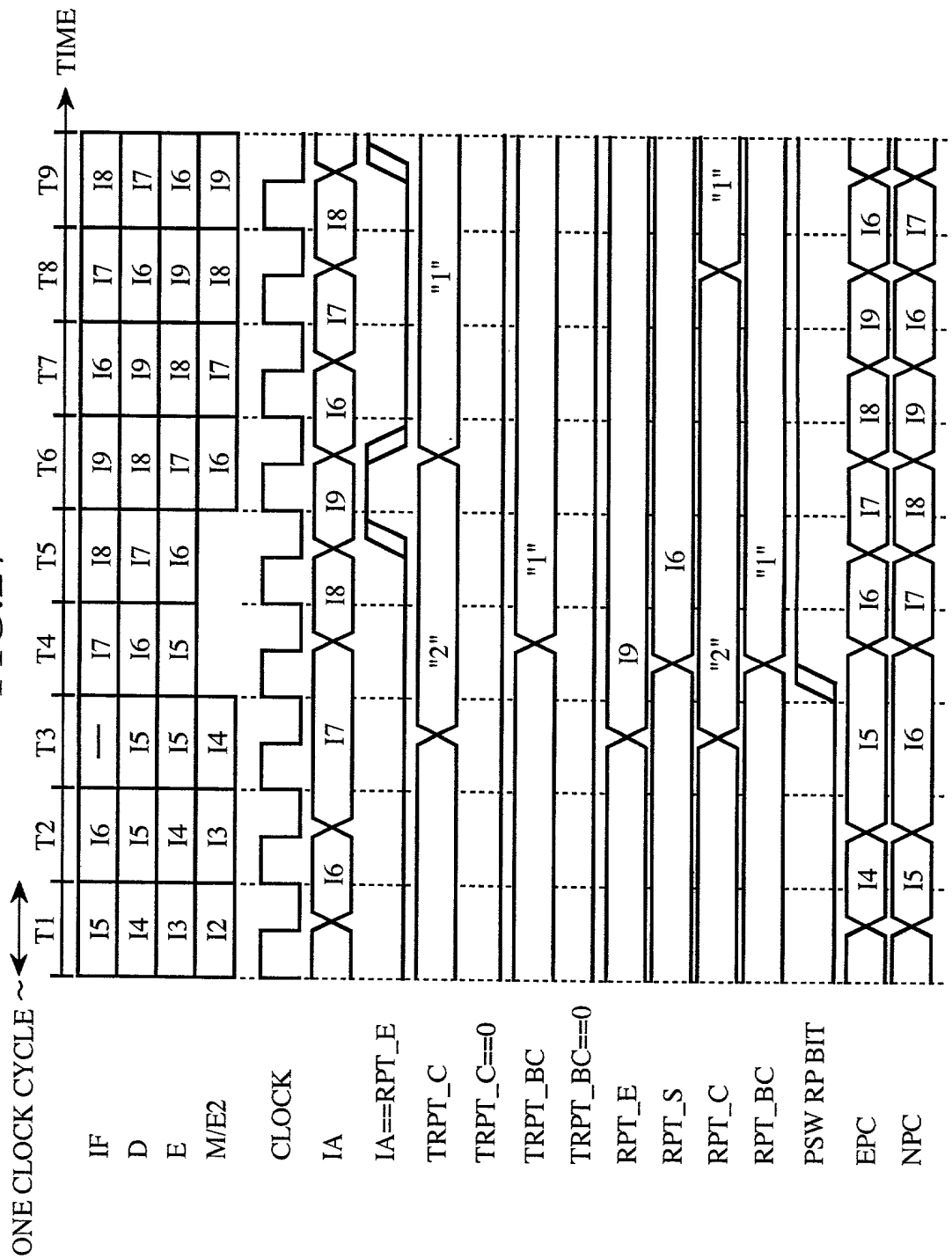
ONE CLOCK CYCLE
T1
T2
T3
T4
T5
T6
T7
T8
T9
TIME
IF
D
E
M/E2
CLOCK
IA
IA==RPT_E
TRPT_C
TRPT_C==0
TRPT_BC
TRPT_BC==0
RPT_E
RPT_S
RPT_C
RPT_BC
PSW RP BIT
EPC
NPC
"1"
"2"

FIG.28

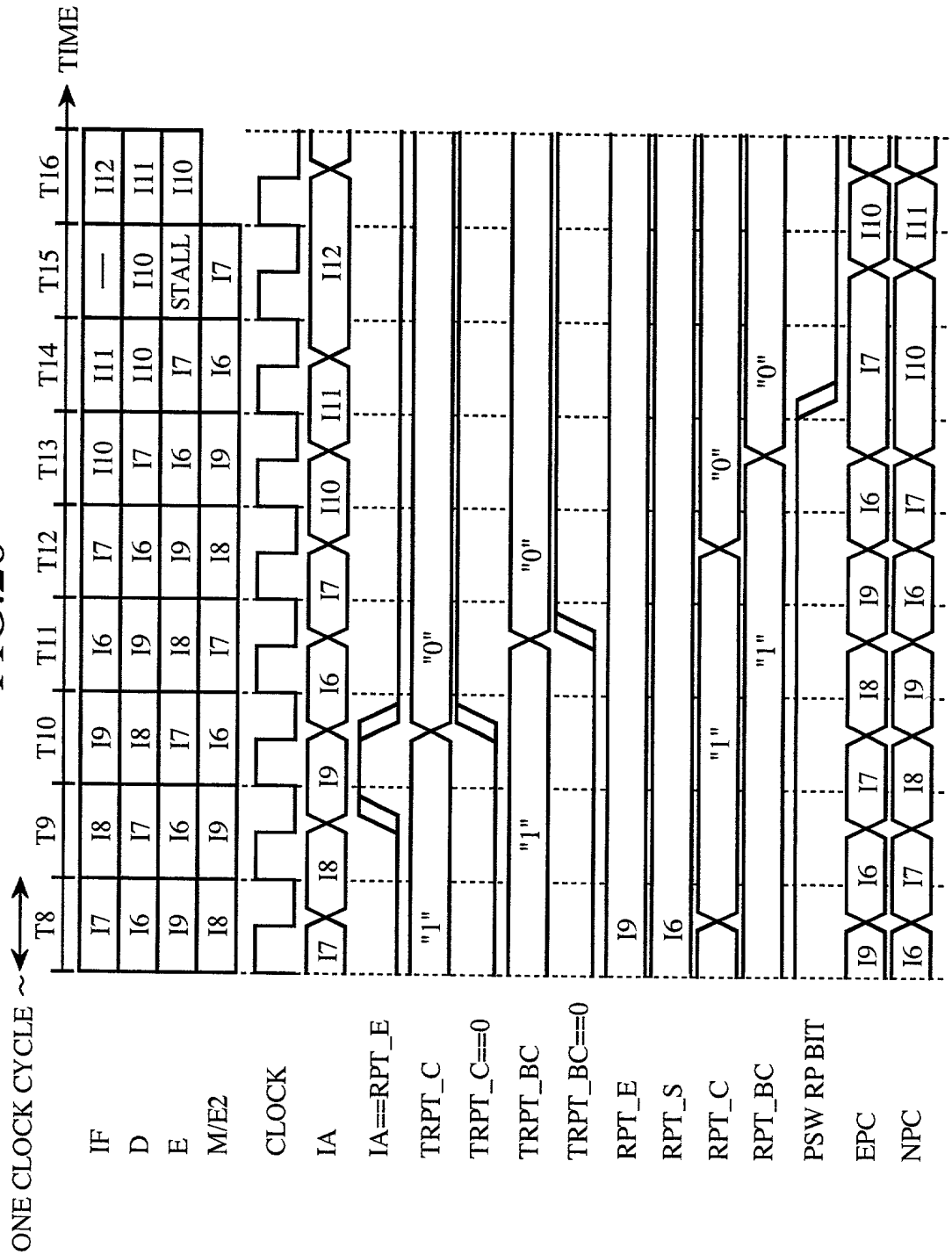
ONE CLOCK CYCLE
T8
T9
T10
T11
T12
T13
T14
T15
T16
TIME
IF
D
E
M/E2
CLOCK
IA
IA==RPT_E
TRPT_C
TRPT_C==0
TRPT_BC
TRPT_BC==0
RPT_E
RPT_S
RPT_C
RPT_BC
PSW RP BIT
EPC
NPC
I7
I8
I9
I6
I10
I11
I12
STALL
"1"
"0"

FIG.30

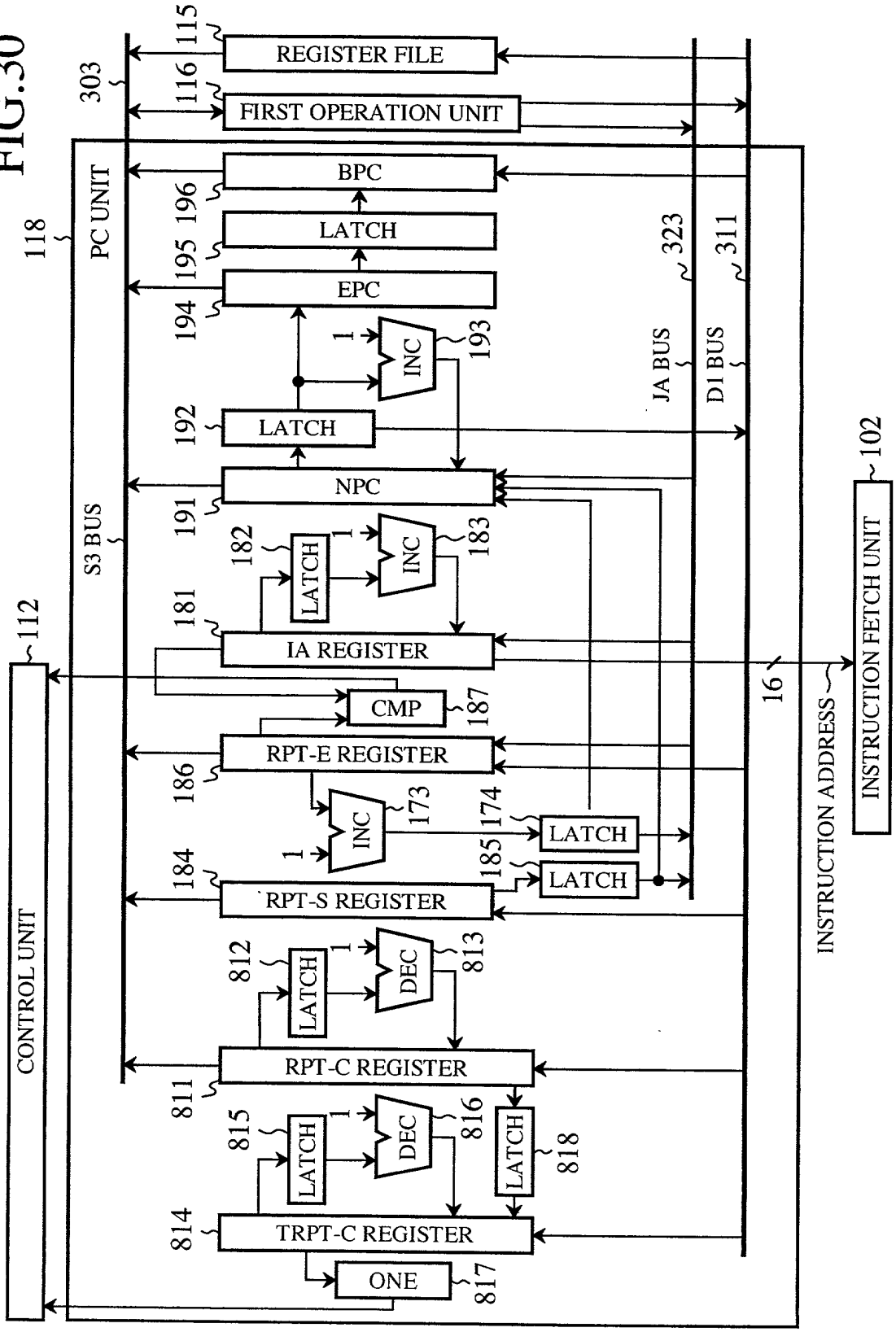
REGISTER FILE
FIRST OPERATION UNIT
BPC
LATCH
EPC
INC
LATCH
NPC
LATCH
INC
IA REGISTER
CMP
RPT-E REGISTER
INC
LATCH
LATCH
RPT-S REGISTER
LATCH
DEC
RPT-C REGISTER
LATCH
DEC
LATCH
TRPT-C REGISTER
ONE
PC UNIT
S3 BUS
JA BUS
D1 BUS
CONTROL UNIT
INSTRUCTION ADDRESS
INSTRUCTION FETCH UNIT
115
116
303
118
196
195
194
193
192
323
311
191
182
183
181
112
187
186
173
174
185
184
812
813
811
815
816
818
814
817
102
16

FIG.31

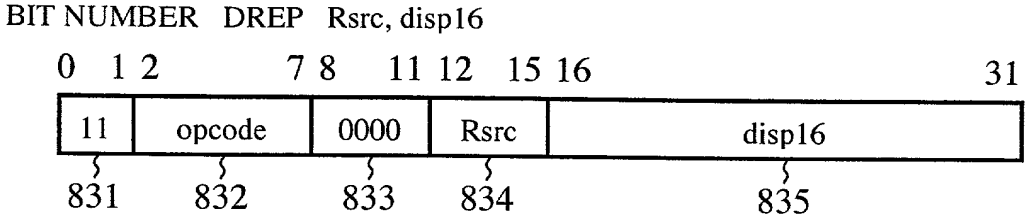

FIG.32

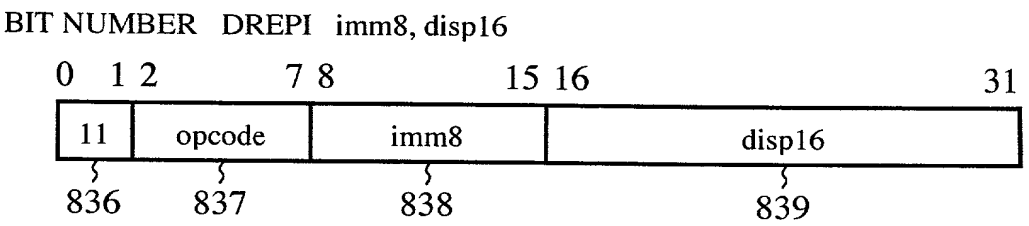

FIG.33

```
    LD2W    R0,@R8+                              ; I1a
    LD2W    R4,@R9+                              ; I1b

    DREP    R10,rep_end                          ; I2

    LD2W    R2,@R8+      ||  CLRAC   A0          ; I3

rep_start :

    LD2W    R6,@R9+      ||  MAC     A0,R0,R4    ; I4
    LD2W    R0,@R8+      ||  MAC     A0,R1,R5    ; I5
    LD2W    R4,@R9+      ||  MAC     A0,R2,R6    ; I6
rep_end :
    LD2W    R2,@R8+      ||  MAC     A0,R3,R7    ; I7

    RACHI   R0,A0,#0     ||  NOP                 ; I8
    :                                            ; I9
    :                                            ; :
```

FIG.34

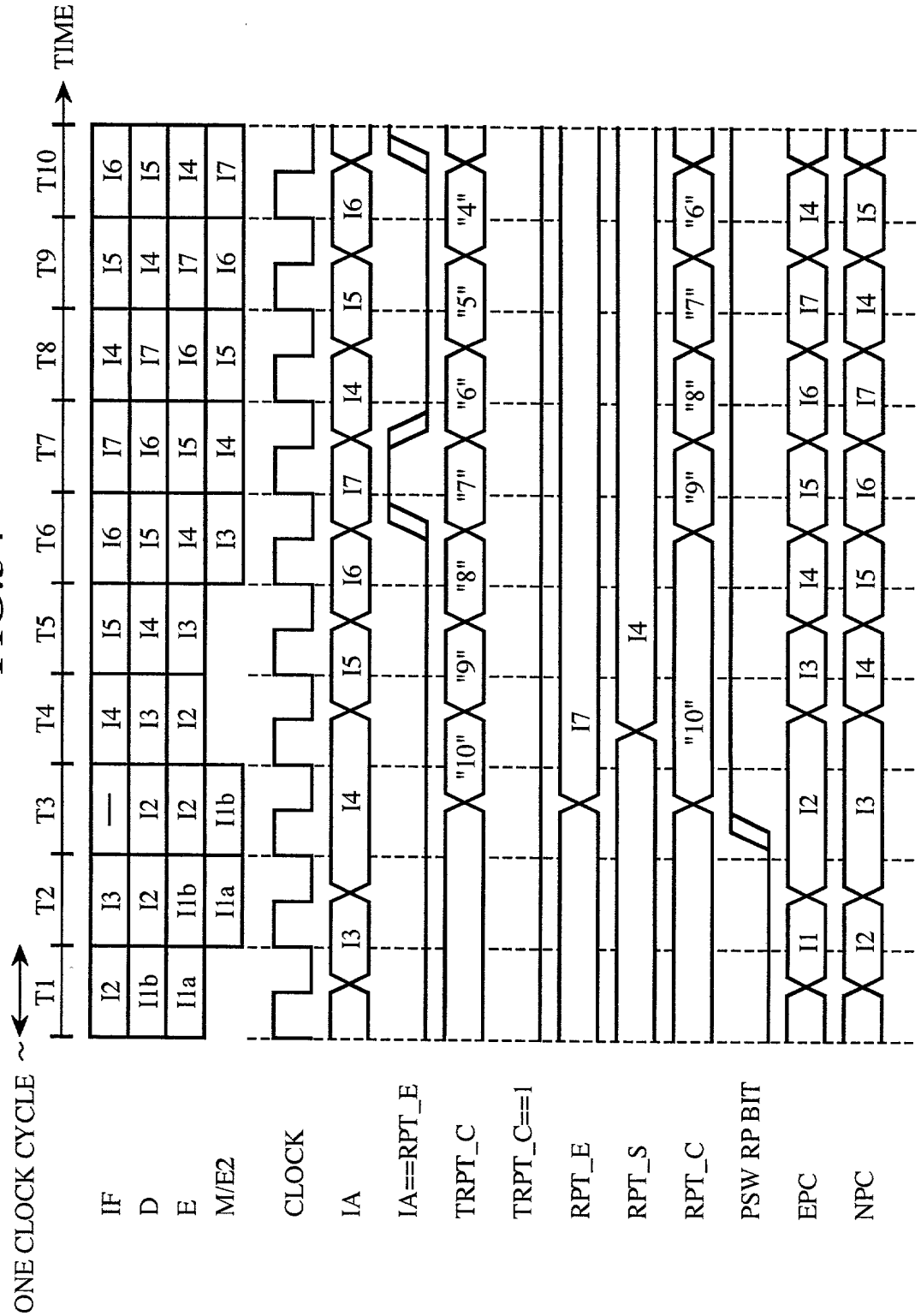
ONE CLOCK CYCLE
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
TIME
IF
D
E
M/E2
CLOCK
IA
IA==RPT_E
TRPT_C
TRPT_C==1
RPT_E
RPT_S
RPT_C
PSW RP BIT
EPC
NPC

FIG.35

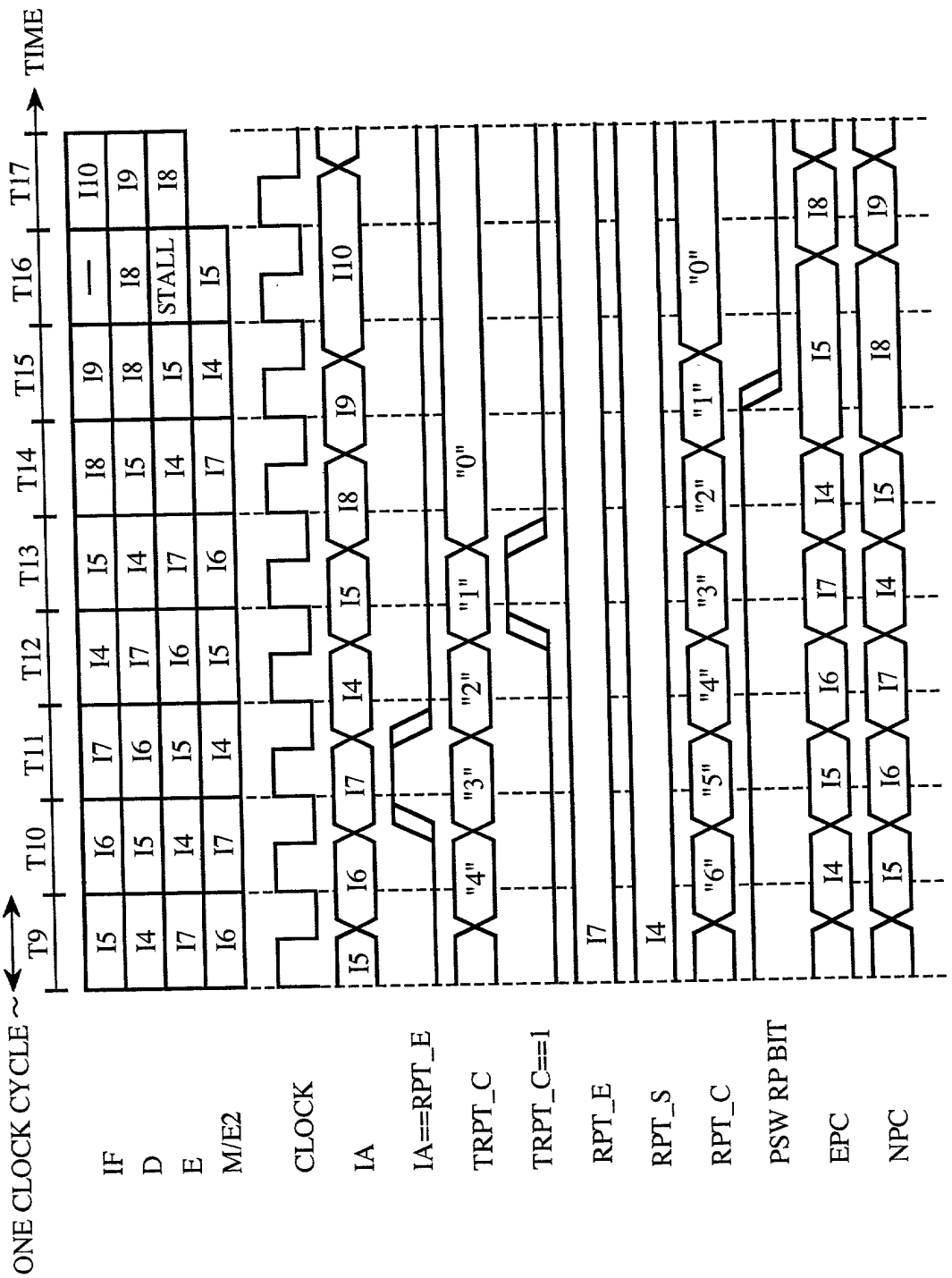
ONE CLOCK CYCLE
T9
T10
T11
T12
T13
T14
T15
T16
T17
TIME
IF
D
E
M/E2
CLOCK
IA
IA==RPT_E
TRPT_C
TRPT_C==1
RPT_E
RPT_S
RPT_C
PSW RP BIT
EPC
NPC
I5
I6
I7
I4
I8
I9
I10
STALL
—
"0"
"1"
"2"
"3"
"4"
"5"
"6"

FIG.36 (PRIOR ART)